National Semiconductor

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LMH6572
Triple 2:1 High Speed Video Multiplexer

General Description

The LMH™6572 is a high performance analog mulitplexer optimized for professional grade video and other high fidelity high bandwidth analog applications. The LMH6572 provides a 290MHz bandwidth at 2 V_{PP} output signal levels. The 140 MHz of .1 dB bandwidth and a 1500 V/µs slew rate make this part suitable for High Definition Television (HDTV) and High Resolution Multimedia Video applications.

The LMH6572 supports composite video applications with its 0.02% and 0.02˚ differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75Ω load. The LMH6572 can deliver 80 mA linear output current for driving multiple video load applications.

The LMH6572 has an internal gain of two for driving back terminated transmission lines at a net gain of one.

The LMH6572 is available in the SSOP package.

Features

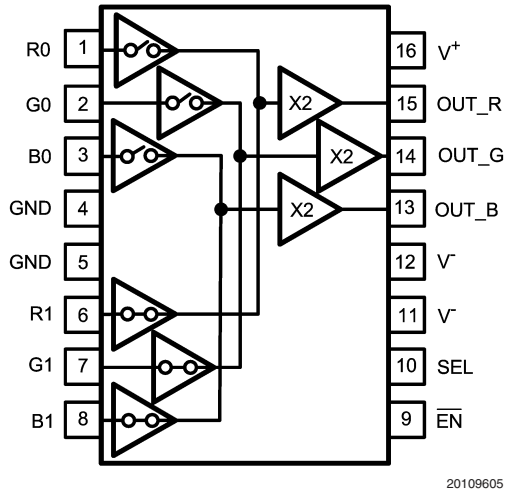
- 350 MHz, 250 mV –3 dB bandwidth
- 290 MHz, 2 V_{PP} –3 dB bandwidth
- 10 ns channel switching time
- 90 dB channel to channel isolation @ 5 MHz
- 0.02%, 0.02˚ diff. gain, phase
- .1 dB gain flatness to 140 MHz
- 1400 V/µs slew rate
- Wide supply voltage range: 6V (±3V) to 12V (±6V)
- –78 dB HD2 @ 10MHz
- –75 dB HD3 @ 10MHz

Applications

- RGB video router
- Multi input video monitor
- Fault tolerant data switch

Connection Diagram

16-Pin SSOP



20109605

Top View

Truth Table

SEL	$\overline{EN}$	OUT
0	0	CH 1
1	0	CH 0
X	1	Disable

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin SSOP	LMH6572MQ	LH6572MQ	95 Units/Rail	MQA16
	LMH6572MQX		2.5 Units Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	(Note 4)
Human Body Model	2000V
Machine Model	200V
Supply Voltage ($V^+ - V^-$)	13.2V
I_{OUT} (Note 3)	130 mA
IInput Voltage Range	$\pm V_S$
Maximum Junction Temperature	+150˚C (Note 4)
Storage Temperature Range	–65˚C to +150˚C
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C

Operating Ratings (Note 1)

Operating Temperature	–40˚C	to	85˚C
Supply Voltage Range	6V	to	12V
Thermal Resistance			
Package	(θ_{JA})		(θ_{JC})
16-Pin SSOP	125˚C/W		36˚C/W

±5V Electrical Characteristics

V_S = ±5V, R_L = 100Ω, Unless otherwise specified.

Symbol	Parameter	Conditions(Note 2)	Min	Typ	Max	Units
Frequency Domain Performance						
SSBW	–3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		350		MHz
LSBW	–3 dB Bandwidth (Note 6)	V_{OUT} = 2 V_{PP}	250	290		MHz
.1 dBBW	. 1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		140		MHz
DG	Differential Gain	R_L = 150Ω, f=4.43 MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, f=4.43 MHz		0.02		deg
Time Domain Response						
TRS	Channel to Channel Switching Time	Logic transition to 90% output		10		ns
	Enable and Disable Times	Logic transition to 90% or 10% output.		11		ns
TRL	Rise and Fall Time	2V Step		1.5		ns
TSS	Settling Time to 0.05%	2V Step		17		ns
OS	Overshoot	4V Step		5		%
SR	Slew Rate(Note 6)	4V Step	1200	1400		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP} , 10 MHz		–78		dBc
HD3	3rd Harmonic Distortion	2 V_{PP} , 10 MHz		–75		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2Vpp at output		–80		dBc
Equivalent Input Noise						
VN	Voltage	>1 MHz, Input Referred		5		nV $\sqrt{Hz}$
ICN	Current	>1 MHz, Input Referred		5		pA/ $\sqrt{Hz}$
Static, DC Performance						
GAIN	Voltage Gain (Note 5)	No Load	1.9	2.0	2.1	V/V
	Gain Error(Note 5)	No Load, channel to channel		±0.3	±0.5 **±0.7**	%
	Gain Error	R_L = 50Ω		0.3		%
VIO	Output Offset Voltage (Note 5)	V_{IN} = 0V		1	±14 **±17.5**	mV
DVIO	Average Drift			27		µV/˚C
IBN	Input Bias Current (Notes 7, 5)	V_{IN} = 0V		–1.4	±2.8 **±3.5**	µA
DIBN	Average Drift			7		nA/˚C
PSRR	Power Supply Rejection Ratio (Note 5)	DC, Input referred	50 **48**	54		dB

±5V Electrical Characteristics (Continued)

V_S = ±5V, R_L = 100Ω, Unless otherwise specified.

Symbol	Parameter	Conditions(Note 2)	Min	Typ	Max	Units
ICC	Supply Current (Note 5)	No Load	20	23	25 **28.5**	mA
	Supply Current Disabled(Note 5)	No Load		2.0	2.2 **2.3**	mA
VIH	Logic High Threshold(Note 5)	Select & Enable Pins	2.0			V
VIL	Logic Low Threshold (Note 5)	Select & Enable Pins			0.8	V
IiL	Logic Pin Input Current Low(Note 7)	Logic Input = 0V		–1	±2.5 **±10**	µA
IiH	Logic Pin Input Current High(Note 7)	Logic Input = 2.0V	112 **100**	150	200 **210**	µA
Miscellaneous Performance						
RF	Internal Feedback and Gain Set resistor Values		650 **620**	800	940 **1010**	Ω
RODIS	Disabled Output Resistance	Internal Feedback and Gain Set resistors in series to ground.	1.3	1.6	1.88	kΩ
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.26		Ω
VO	Output Voltage Range	No Load	±3.83 **±3.80**	±3.9		V
VOL		R_L = 100Ω	±3.52 **±3.5**	±3.53		V
CMIR	Input Voltage Range		±2	±2.5		V
IO	Linear Output Current (Notes 5, 7)	V_{IN} = 0V,	+70 -40	±80		mA
ISC	Short Circuit Current	V_{IN} = ±2V, Output shorted to ground		±230		mA
XTLK	Channel to Channel Crosstalk	V_{IN} = 2 V_{PP} @5 MHz		–90		dBc
XTLK	Channel to Channel Crosstalk	V_{IN} = 2 V_{PP} @ 100 MHZ		–54		dBc
XTLK	All Hostile Crosstalk	In A, C. Out B, V_{IN} = 2 V_{PP} @ 5 MHz		–95		dBc

±3.3V Electrical Characteristics

V_S = ±3.3V, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions(Note 2)	Min	Typ	Max	Units
Frequency Domain Performance						
SSBW	–3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		360		MHz
LSBW	–3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		270		MHz
.1 dBBW	.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		80		MHz
GFP	Peaking	DC to 200 MHz		0.3		dB
DG	Differential Gain	R_L = 150Ω, f=4.43 MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, f=4.43 MHz		0.03		deg
Time Domain Response						
TRS	Rise and Fall Time	2V Step		2.0		ns
TSS	Settling Time to 0.05%	2V Step		15		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	2V Step		1000		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10MHz		–70		dBc

±3.3V Electrical Characteristics (Continued)

V_S = ±3.3V, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions(Note 2)	Min	Typ	Max	Units
HD3	3rd Harmonic Distortion	2 V_{PP}, 10MHz		–74		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2Vpp at output		–79		dBc
Static, DC Performance						
GAIN	Voltage Gain			2.0		V/V
VIO	Output Offset Voltage	V_{IN} = 0V		1		mV
DVIO	Average Drift			36		µV/˚C
IBN	Input Bias Current (Note 7)	V_{IN} = 0V		2		µA
DIBN	Average Drift			24		nA/˚C
PSRR	Power Supply Rejection Ratio	DC, Input Referred		54		dB
ICC	Supply Current	R_L = ∞		20		mA
VIH	Logic High Threshold	Select & Enable Pins			1.3	V
VIL	Logic Low Threshold	Select & Enable Pins	0.4			V
Miscellaneous Performance						
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.27		Ω
VO	Output Voltage Range	No Load		±2.5		V
VOL		R_L = 100Ω		±2.2		V
CMIR	Input Voltage Range			±1.2		V
IO	Linear Output Current	V_{IN} = 0V		±60		mA
ISC	Short Circuit Current	V_{IN} = ±1V, Output shorted to ground		±150		mA
XTLK	Channel to Channel Crosstalk	5 MHz		–90		dBc

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details. A short circuit condition should be limited to 5 seconds or less.

Note 4: Human Body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω In series with 200 pF

Note 5: Parameters guaranteed by electrical testing at 25˚ C.

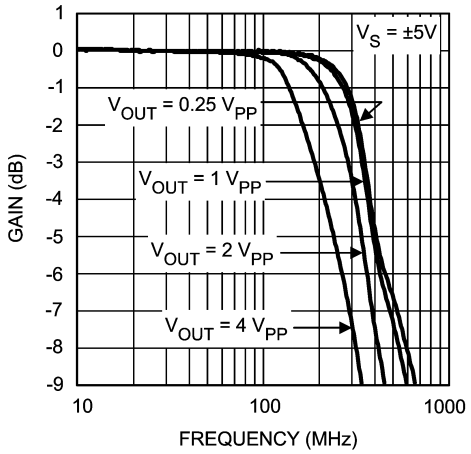
Note 6: Parameters guaranteed by design.

Note 7: Positive Value is current into device.

Typical Performance Characteristics

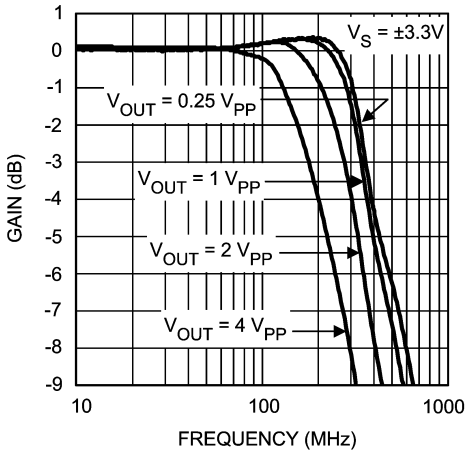
V_s = ±5V, R_L = 100Ω; unless otherwise specified.

Frequency Response vs. V_{OUT}



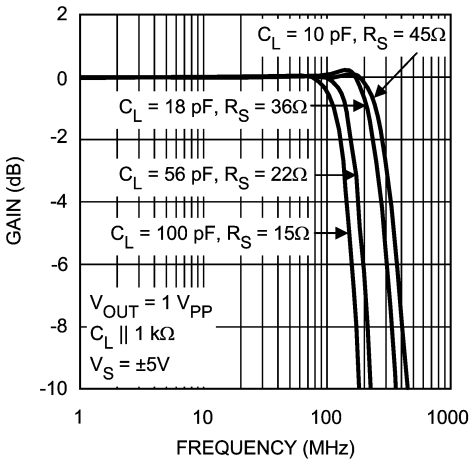
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Frequency Response vs. V_{OUT}



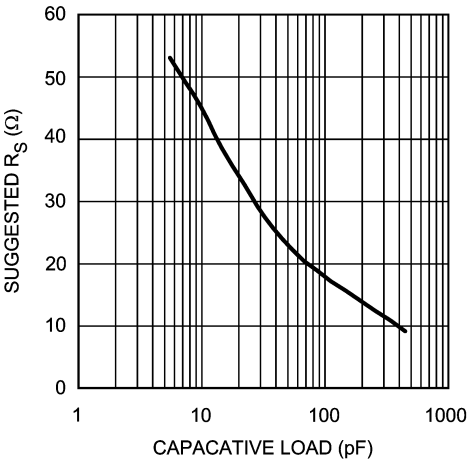
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Frequency Response vs. Capacitive Load



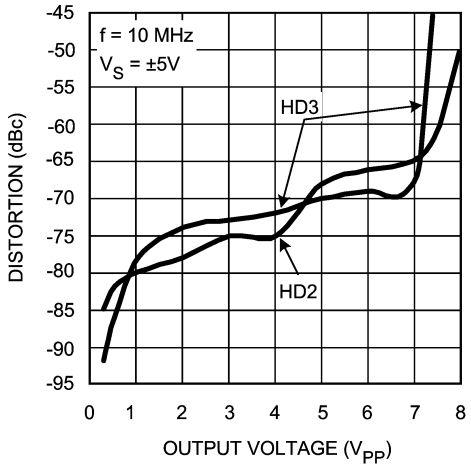
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Suggested R_S vs. Capacitive Load
Load= 1kΩ ‖ C_L



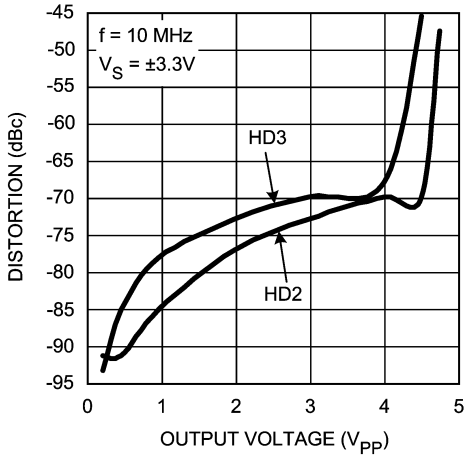
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Harmonic Distortion vs. Output Voltage



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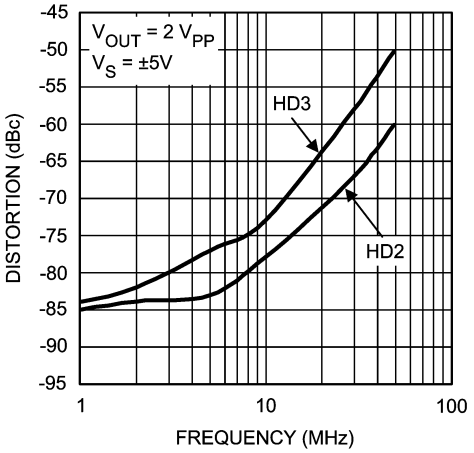
Harmonic Distortion vs. Output Voltage



20109612

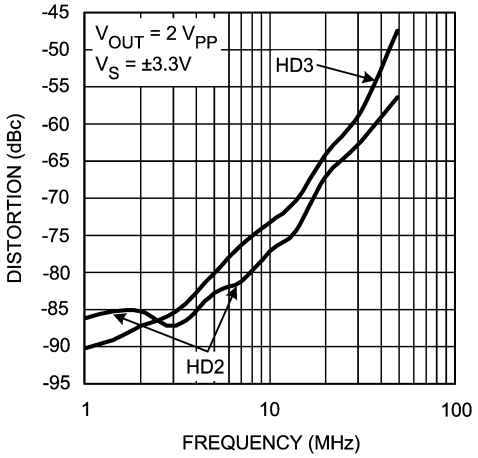
Typical Performance Characteristics V_s = ±5V, R_L = 100Ω; unless otherwise specified. (Continued)

Harmonic Distortion vs. Frequency



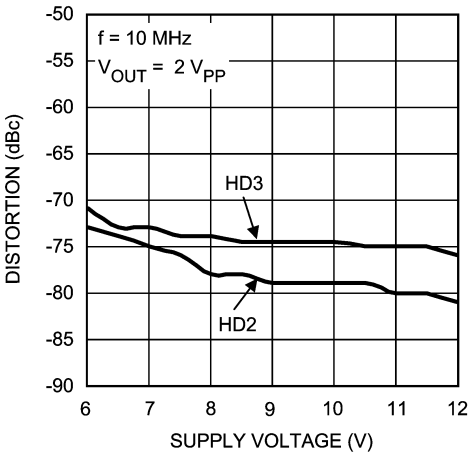
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Harmonic Distortion vs. Frequency



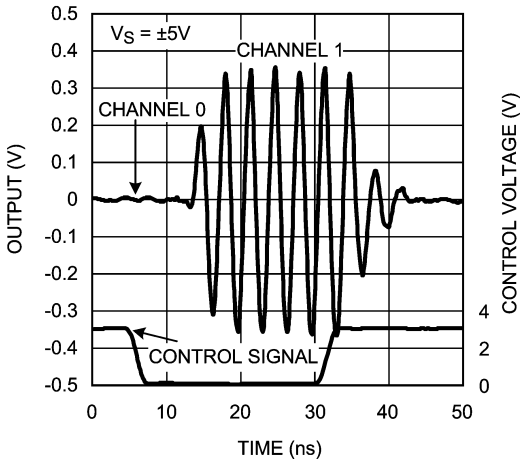
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Harmonic Distortion vs. Supply Voltage



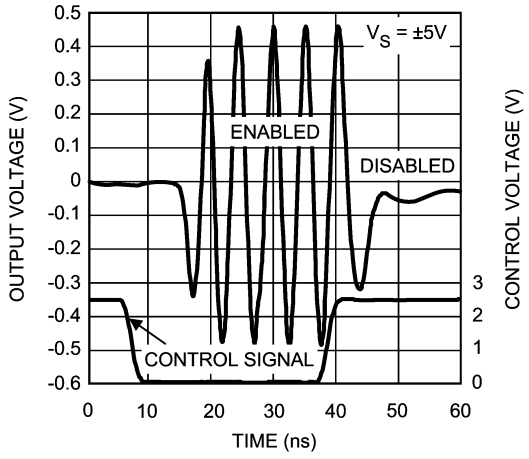
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Channel Switching Time



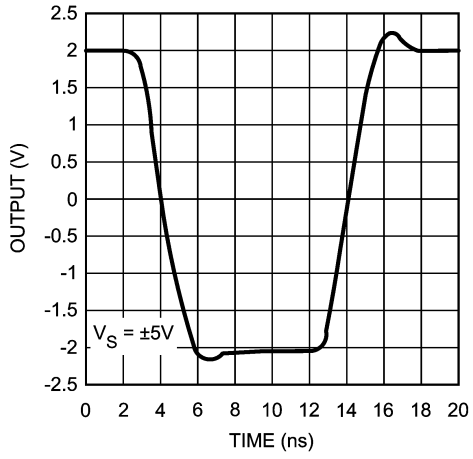
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Disable Time



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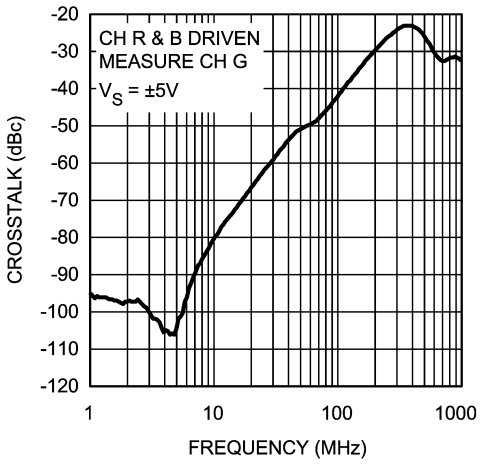
Pulse Response



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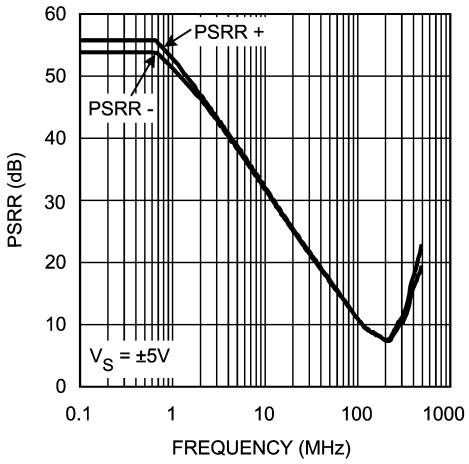
Typical Performance Characteristics V_s = ±5V, R_L = 100Ω; unless otherwise specified. (Continued)

Crosstalk



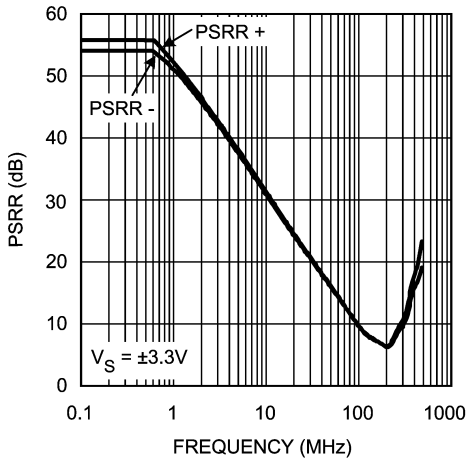
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PSRR



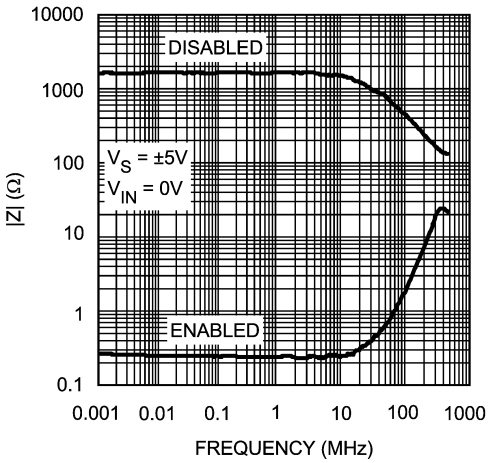
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PSRR



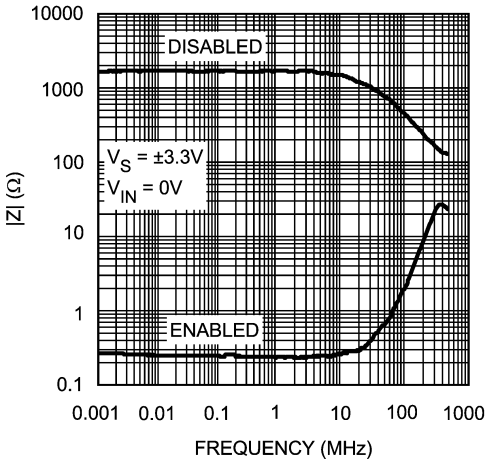
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Closed Loop Output Impedance



20109609

Closed Loop Output Impedance



20109608

Application Notes

GENERAL INFORMATION

The LMH6572 is a high-speed triple 2:1 multiplexer, optimized for very high speed and low distortion. With a fixed gain of 2 and excellent AC performance, the LMH6572 is ideally suited for switching high resolution, presentation grade video signals. The LMH6572 has no internal ground reference. Single or split supply configurations are both possible. The LMH6572 features very high speed channel switching and disable times. When disabled the LMH6572 output is high impedance making MUX expansion possible by combining multiple devices.

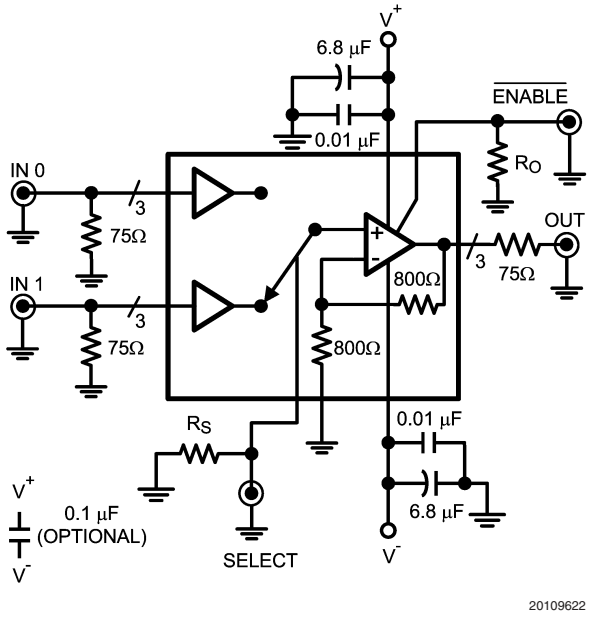


FIGURE 1. Typical Application

VIDEO PERFORMANCE

The LMH6572 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.*Figure 1* shows a typical configuration for driving a 75. Cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

SINGLE SUPPLY OPERATION

The LMH6572 uses mid supply referenced circuits for the select and disable pins. In order to use the LMH6572 in single supply configuration it is necessary to use a circuit similar to *Figure 2*. In this configuration the logical inputs are compatible with high breakdown Open collector TTL, or Open Drain CMOS logic. In addition, the default logic state is reversed since there is a pull up resistor on those pins. Single supply operation also requires the input to be biased to within the common mode input range of roughly ±2V from the mid supply point.

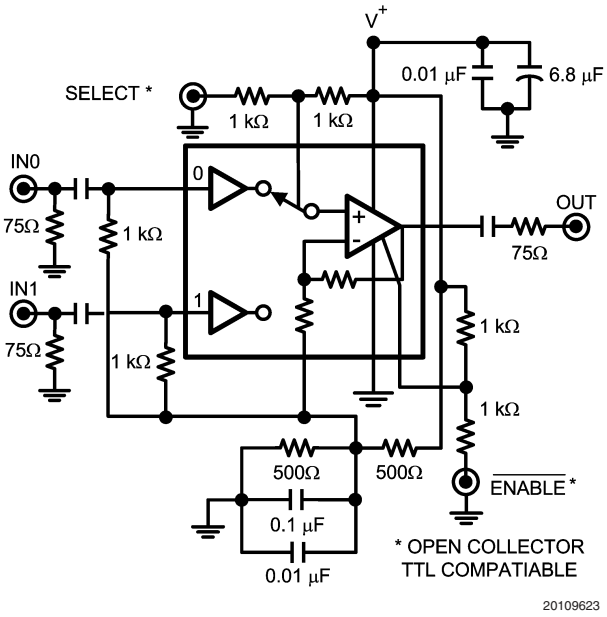


FIGURE 2. Single Supply Application

GAIN ACCURACY

The gain accuracy of the LMH6572 is accurate to ±0.5% (0.3% typical) and stable over temperature. The internal gain setting resistors, R_F and R_G, match very well. However, over process and temperature their absolute value will change.

EVALUATION BOARDS

National Semiconductor provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

Device	Package	Evaluation Board Part Number
LMH6572	TSSOP	LMH730151

An evaluation board is shipped when a sample request is placed with National Semiconductor.

MULTIPLEXER EXPANSION

With the Enable or the Select pins putting the output stage into a high impedance state, several LMH6572's can be tied together to form a larger input MUX. However, there is a slight loading effect on the active output caused by the off-channel feedback and gain set resistors, as shown in *Figure 3* below. *Figure 3* is assuming there are 4 LMH6572 outputs (2 LMH6572 devices) similar to the schematic of *Figure 4*. With the internal resistors valued at 800Ω, the effect is rather slight. For the 4:1 MUX function shown in *Figure 3*, the gain error is only about -0.57 dB, or about 6%.

Application Notes (Continued)

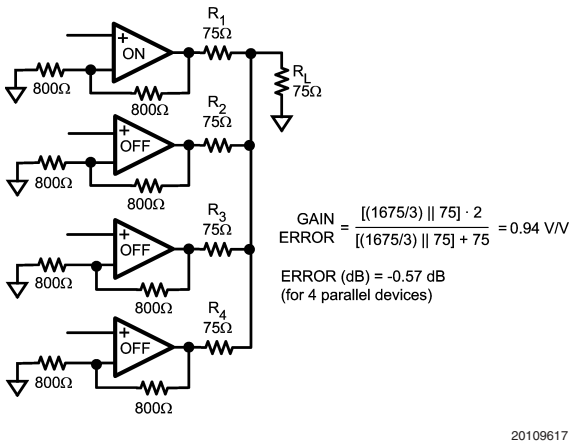


FIGURE 3. Multiplexer Input Expansion by Combining Output

An alternate approach would be to tie the outputs directly together and let all devices share a common back termination resistor in order to alleviate the gain error issue above. The drawback in this case is the increased capacitive load presented to the output of each LMH6572 due to the off-state capacitance of the LMH6572.

EXPANDING THE MUX

It is possible to build higher density MUX's by paralleling several LMH6572's. *Figure 4* shows a 4:1 RGB MUX using two LMH6572's:

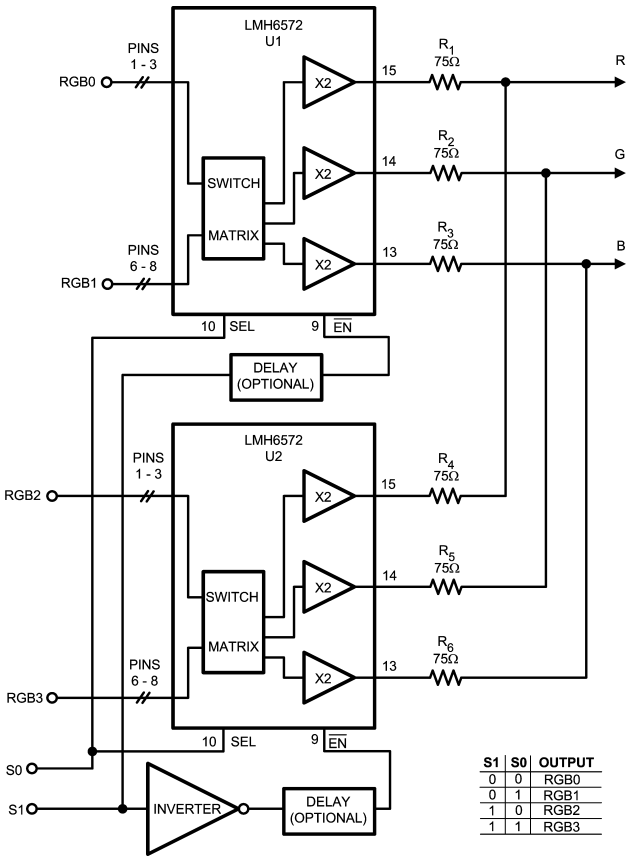


FIGURE 4. RGB MUX USING TWO LMH6572's

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, prior to the $\overline{\text{ENABLE}}$ ($\overline{\text{EN}}$) pin of each device, as shown. *Figure 5* shows one possible approach to this delay circuit. The delay circuit shown will delay $\overline{\text{ENABLE}}$'s H to L transitions (R_1 and C_1 decay) but won't delay its L to H transition.

Application Notes (Continued)

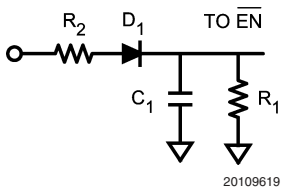


FIGURE 5. Delay Circuit Implementation

R_2 should be kept small compared to R_1 in order to not reduce the $\overline{\text{ENABLE}}$ voltage and to produce little or no delay to $\overline{\text{ENABLE}}$.

Other Applications

The LMH6572 may be utilized in systems that involve a single RGB channel as well whenever there is a need to switch between different "flavors" of a single RGB input. Here are some examples:

1. RGB positive polarity, negative polarity switch
2. RGB full resolution, High Pass filter switch

In each of these applications, the same RGB input occupies one set of inputs to the LMH6572 and the other "flavor" would be tied to the other input set.

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. *Figure 6* shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart "Suggested R_{OUT} vs. Cap Load" gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

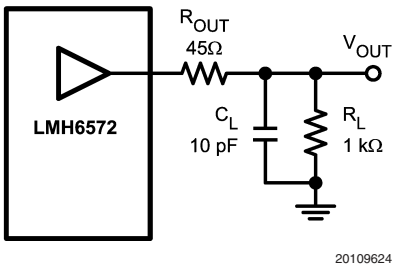


FIGURE 6. Decoupling Capacitive Loads

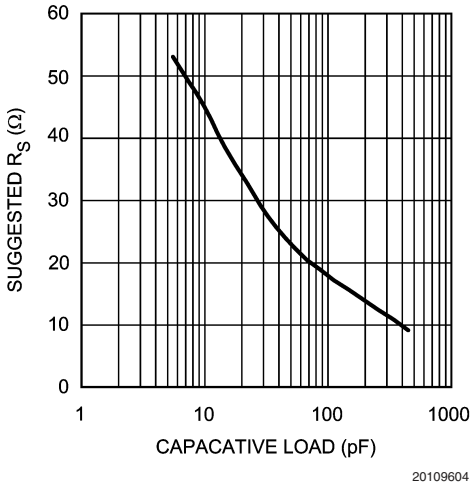


FIGURE 7. Recommended R_{OUT} vs. Capacitive Load

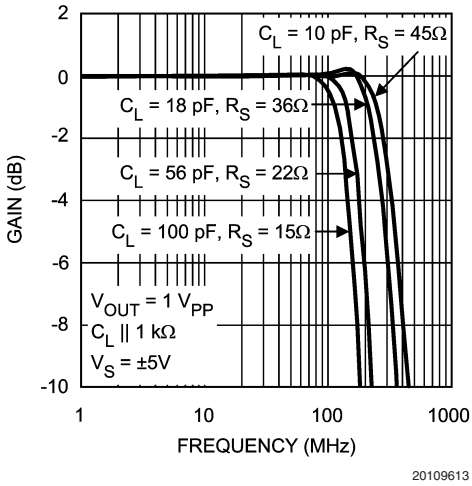


FIGURE 8. Frequency Response vs. Capacitive Load

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730151 is the evaluation board supplied with samples of the LMH6572. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In *Figure 1* and *Figure 2*, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of .01 µF and .1 µF ceramic capacitors for each supply bypass.

Other Applications (Continued)

POWER DISSIPATION

The LMH6572 is optimized for maximum speed and performance in the small form factor of the standard SSOP package. To achieve its high level of performance, the LMH6572 consumes 23 mA of quiescent current, which cannot be neglected when considering the total package power dissipation limit. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6572:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}$* (V_S), where $V_S = V^+ - V^-$.
2. Calculate the RMS power dissipated in the output stage: P_D (rms) = rms (($V_S - V_{OUT}$) * I_{OUT}), where V_{OUT} and I_{OUT} are the voltage across and the current through the external load and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6572, package can dissipate at a given temperature can be derived with the following equation:

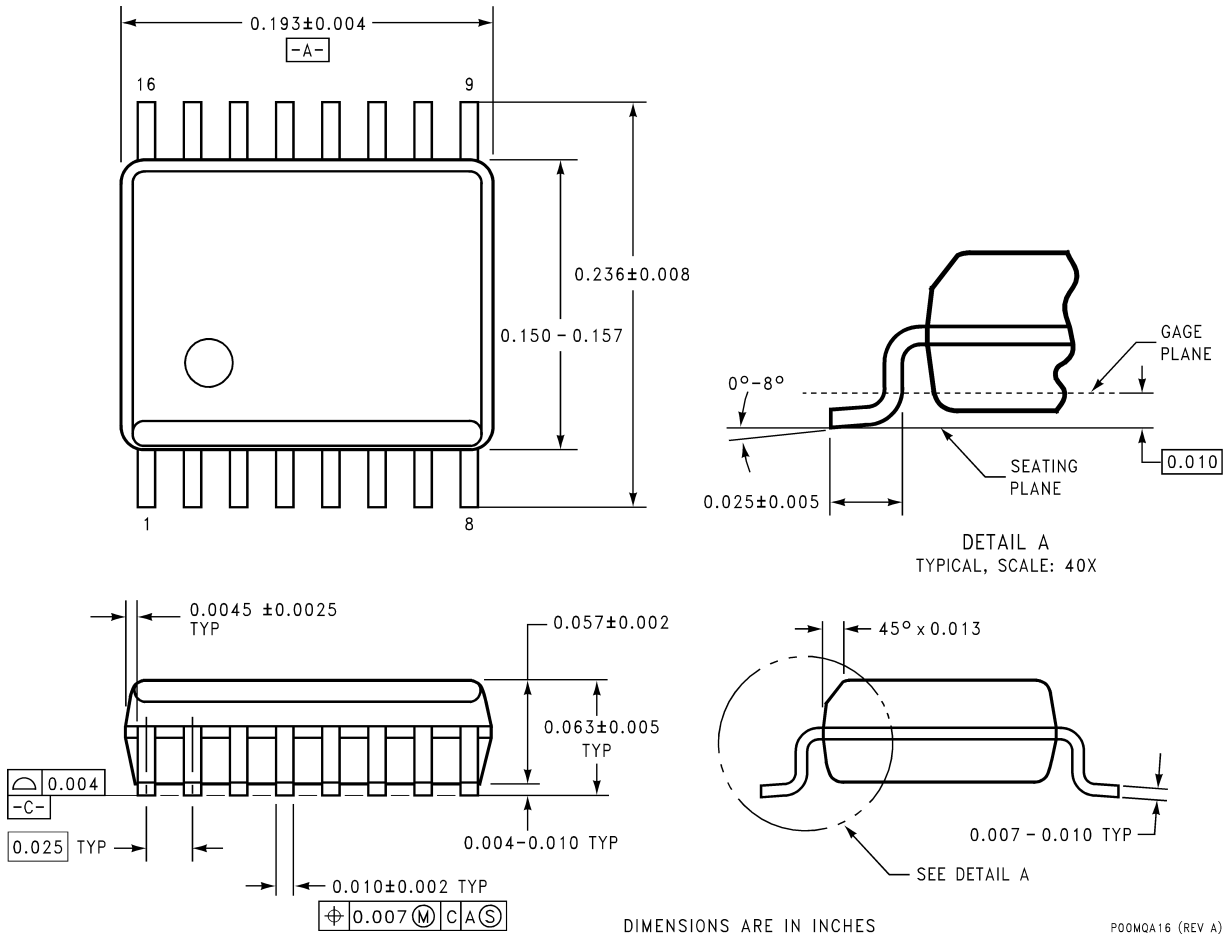
$P_{MAX} = (150^\circ - T_{AMB})/ \theta_{JA}$, where T_{AMB} = Ambient temperature (˚C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (˚C/W). For the SSOP package θ_{JA} is 125˚C/W.

ESD PROTECTION

The LMH6572 is protected against electrostatic discharge (ESD) on all pins. The LMH6572 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6572 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

Physical Dimensions inches (millimeters)

unless otherwise noted



16-Pin SSOP
NS Package Number MQA16

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